SOLID STATE ELECTRONICS LABORATORY

STANFORD ELECTRONICS LABORATORIES
DEPARTMENT OF ELECTRICAL ENGINEERING
STANFORD UNIVERSITY · STANFORD, CA 94305

INVESTIGATION OF METALLIC IMPURITIES INTRODUCED INTO SiO_2 AND SILICON BY VARIOUS CANDIDATE VLSI METALLIZATION SYSTEMS: CHEMICAL REACTIONS, DIFFUSION, AND ELECTRICAL PROPERTIES

FINAL REPORT

CONTRACT NO. MDA 903-82-X-0412

DARPA Order No. A04541

Effective Date of Contract: 06/1/82

Expiration Date of Contract: 30/11/84

Principal Investigators:

T. W. Sigmon and R. M. Swanson
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I. Introduction

The main objectives of this project were to investigate the diffusion of various gate metals into SiO_2, and the diffusion of metals into silicon from contact metalization. The bulk of the work was performed on SiO_2, and experimental diffusion results were obtained for Ag, Cu, Pd, Au, Ta, and Ti. From these results, a model for interstitial diffusion in SiO_2 was developed that predicts both the ionization state and activation energy for diffusion and solid solubility as a function of temperature. The work concluded that Pd, Au, Mo, Ta, W, Pt, Ti, and Al are suitable candidates for VLSI gate and interconnect metalizations, whereas Ag, Cu, Na, Ni, Mn, Fe, Mg, and Ga are not.

This report covers work performed to detect and measure the diffusion of contact metals into crystalline Si. This effort encountered more experimental problems than the SiO_2 case, partially because in VLSI technology there are both different types of contacts and varying junction depths present below the contacts. Realizing the importance of these points enabled us to choose a suitable mask set to take these parameters into account. The parameters of interest in this work are; junction depth, junction conductivity type, overlapped or enclosed junction geometry, and contact metalization. Junctions with different combinations of these parameters are subjected to Bias Current Temperature Stressing (BJTS) at elevated temperatures to simulate a long *Dt* diffusion. The various diodes are packaged to avoid direct probing, and to make sure the temperature is constant for all the diodes undergoing BJTS.

II. Experimental Approach

The experimental approach is to perform BJTS on diodes fabricated on the same wafer die. These die are packaged to minimize the effect of the direct probing on the contact. Fig. 1 shows the diode mask. Note that these diodes are actually rows of contacts consisting of 1, 5, 25 and 125 rows each containing 76 contacts per row. In this way surface area diffusion effects can be separated from perimeter or edge effects. Fig. 2 shows the two types of contact structures available on this mask set. The enclosed contact structure is in general more reliable, but has layout and processing disadvantages when compared to the overlapped contact. The main layout disadvantage is that they need to be made larger than the overlapped contacts because of the tight lithography requirements of placing a square inside of another square. These structures, when combined with the different numbers of contacts per diode, enable us to obtain data on diodes with from 76 to 9500 contacts for both the enclosed and overlapped p^+/n and

n^+/p cases.

The experimental set up is shown in Fig. 3(a) and is basically the same furnace and boat used in the gate-metalization portion of the work. (See Mid-Term Technical Report 9/1/82-9/31/83.) Some modifications of the boat were necessary in order to bias the diodes in forward and reverse bias for both the n^+/p and the p^+/n cases. The typical experimental connections and locations of the packaged diodes on the boat are shown in Fig. 3(b). Each BJTS run thus has both aluminum and platinum metalization for all diode types during the same experiment. In this manner the results can be correlated in a "constant experiment" approach. The electrical connections are made so that diodes of the same size receive the same bias. The four sizes of diodes are numbered 1 through 4 with sizes 1 and 4 receiving no bias while diode 2 receives forward bias at 0.3 volts, and diode 3 receiving a reverse bias of -5 volts. Since the CMOS process calls for p-type wafers with n-wells to define the p-channel devices, there is no way to reverse bias the n-channel diodes without producing a latch-up condition. It is therefore necessary to omit the -5 volts on the n^+/p diodes while the p^+/n diodes are biased to +5 volts reverse bias. A summary of these connections has been given in Fig. 1.

A BJTS run consists of connecting the packaged diodes as shown in Fig. 3(b) and introducing the boat into the room temperature furnace in a flowing forming gas ambient. The power is then turned on and the temperature rapidly increased to 300 °C. This procedure is necessary to avoid oxidation of the tungsten probes. After 3 hours at between 300 and 310 °C the furnace power is turned off and the temperature allowed to decrease back to room temperature. A typical time versus temperature plot is shown in Fig. 4.

III. Results and Conclusions

The experiment intends to examine the behavior of the overlapped contacts and enclosed contacts to determine if metal diffusion is primarily a bulk effect, which would tend to degrade both types of contacts, or a Si-SiO_2 boundary diffusion problem, which would degrade only the overlapped contacts for our biasing conditions. There is no plethoria of literature on these types of experiments so the results are important to analyze for VLSI reliability studies.

Diode data is taken before and after BJTS to insure that the diodes are well behaved before the BJTS, and to directly correlate I-V differences after the stress. In general the diodes are well behaved, an exception being the n^+/p overlapped diodes which failed for both aluminum and platinum metalization before BJTS. All other diode

types, namely the enclosed n^+/p, overlapped p^+/n, and enclosed p^+/n for either aluminum or platinum metalization showed ideal diode behavior with $\eta \sim 1$ before BJTS.

In the following discussion the results for each type of contact are presented, and correlations made. The first type of contact to be considered is the overlapped n^+/p. Measurements made before BJTS show that all of these contacts were punched through during processing. This may be due to the fact that the n^+ junction depth is shallow ($<0.3\mu$m) and diffusion of the metal along the SiO_2/n^+-Si interface during the sintering step is sufficient to spike the junction. The resulting I-V curve shows linear behavior dominated by the series resistance of the substrate. Of course, measurements made on the diodes after BJTS have the same behavior for both Al and Pt metalizations.

The next type of contact considered is the enclosed n^+/p structure. The data taken before BJTS show well behaved diode log I_d *vs.* V_d curves for both the Al and Pt metalizations. After BJTS there are different results for the two metals. The Al diodes all failed, a typical before and after BJTS curve is shown in Fig. 5(a) for the case of zero bias during BJTS. The results for forward and reverse bias are the same for the 3 hour 300°C BJTS. The Pt diodes, however, exhibited different results. Fig. 5(b) shows a typical before and after BJTS result for an enclosed n^+/p Pt metallized junction. Note there is an increase in leakage current at low bias for the after BJTS case. This indicates that Pt has diffused into the junction resulting in deep levels. These levels act as current generation centers under depletion conditions. Thus, it appears that the Pt has diffused into the junction, but there is no spiking observed as for the Al junctions. The results for the Pt junctions are also bias independent at least for the 3 hour 300°C case.

The p^+/n junctions are not as shallow as the n^+/p junctions due to the difficulty in fabricating shallow boron junctions. This is due to the characteristic channeling tail observed for all energies of implantation. Because of the different conductivity type and depth of these junctions, it is expected that the results for the p^+/n case will be different. The first p^+/n junction results we describe are for the overlapped structures. Data taken before BJTS showed good diode characteristics when compared to the overlapped n^+/p structures which, as previously mentioned, yielded poor I-V characteristics. The Al overlapped p^+/n junctions show no degradation after BJTS except for the forward biased case. Fig. 6(a) shows the increase in leakage current at low forward biases up to 0.6 volts, and the same current thereafter. The Al has diffused significantly into the junction and is apparently at the onset of spiking. The results

obtained for the zero and reverse bias cases show no change in log I_d *vs.* V_d. This is the only case where a bias dependence on the results was seen for the 3 hour 300°C stresses.

The overlapped Pt-p^+/n diodes show interesting results after BJTS. For all polarities there is a marked reduction in current at higher bias. In Fig 6(b) it is seen that the series resistance has increased significantly to limit the junction current. The fact that this is observed for only the overlapped p^+/n structure indicates this is an SiO_2/p^+-Si boundary phenomenon. More studies to isolate this problem are needed in order to characterize this result sufficiently.

The enclosed p^+/n structures are the least effected by BJTS. Measurements taken before and after BJTS show identical behavior for both Al and Pt diodes except for the forward bias Al case. As for the case for the overlapped p^+/n structure, there is an increase in leakage for the forward bias case up to about 0.6 volts although the leakage is only slighlty higher than that measured for the enclosed structure. This result is shown in Fig. 7. These results tend to support the conjecture that Al diffuses as a positive ion in Si. In addition, the fact that all of the other diodes are not affected by BJTS indicates that deeper junctions are more tolerant to metal diffusion than shallower ones. Since the push in today's technology is for very shallow junctions, on the order of 0.1 to 0.15 μm, it is important to understand the diffusion mechanisms of these and other metals used for these contact structures.

In summary the enclosed structures are less affected, and therefore, appear to be more reliable than the overlapped structures. In addition, the p^+/n diodes are better after BJTS than the n^+/p this being most likely due to their deeper junction depth. For the n^+/p diodes, none of the overlapped junctions work following sinter which indicates a need for more controlled processing of these structures for VLSI applications. The enclosed structures all failed, although the characteristic failure appears to be different for Al than for Pt. The Pt diodes showing only increased leakage at low forward bias while the Al diodes spike the junction. For the p^+/n diodes, the overlapped case has the most interesting results, the Al diodes are only affected for forward bias, while the Pt diodes show a dramatic increase in the series resistance of the junction. The enclosed case shows unchanged behavior after BJTS for both the Al and Pt except for the forward bias BJTS Al case.

IV. Future Work

The results obtained here for the diffusion of Al and Pt into Si from contacts are preliminary at best. Further work needs to be performed before a cohesive

understanding of the diffusion mechanisms of these and other metals will be known. Although work is no longer funded by DARPA at Stanford, perhaps, the results will help future work in this area by other researchers. One significant contribution to the actual experimental set is the realization that BJTS experiments are best carried out in ovens that have maximum temperatures of ~400°C and not necessarily the type of furnace used in these experiments. This furnace was used to maintain a "constant experiment" environment for the metal-SiO_2 and metal-Si systems. It would be more efficient if the packaged diodes were plugged into circuit boards that can be connected to external power supplies. In this manner the devices can be tested without probing, resulting in an ease of setting up the experiment that was absent for our case.

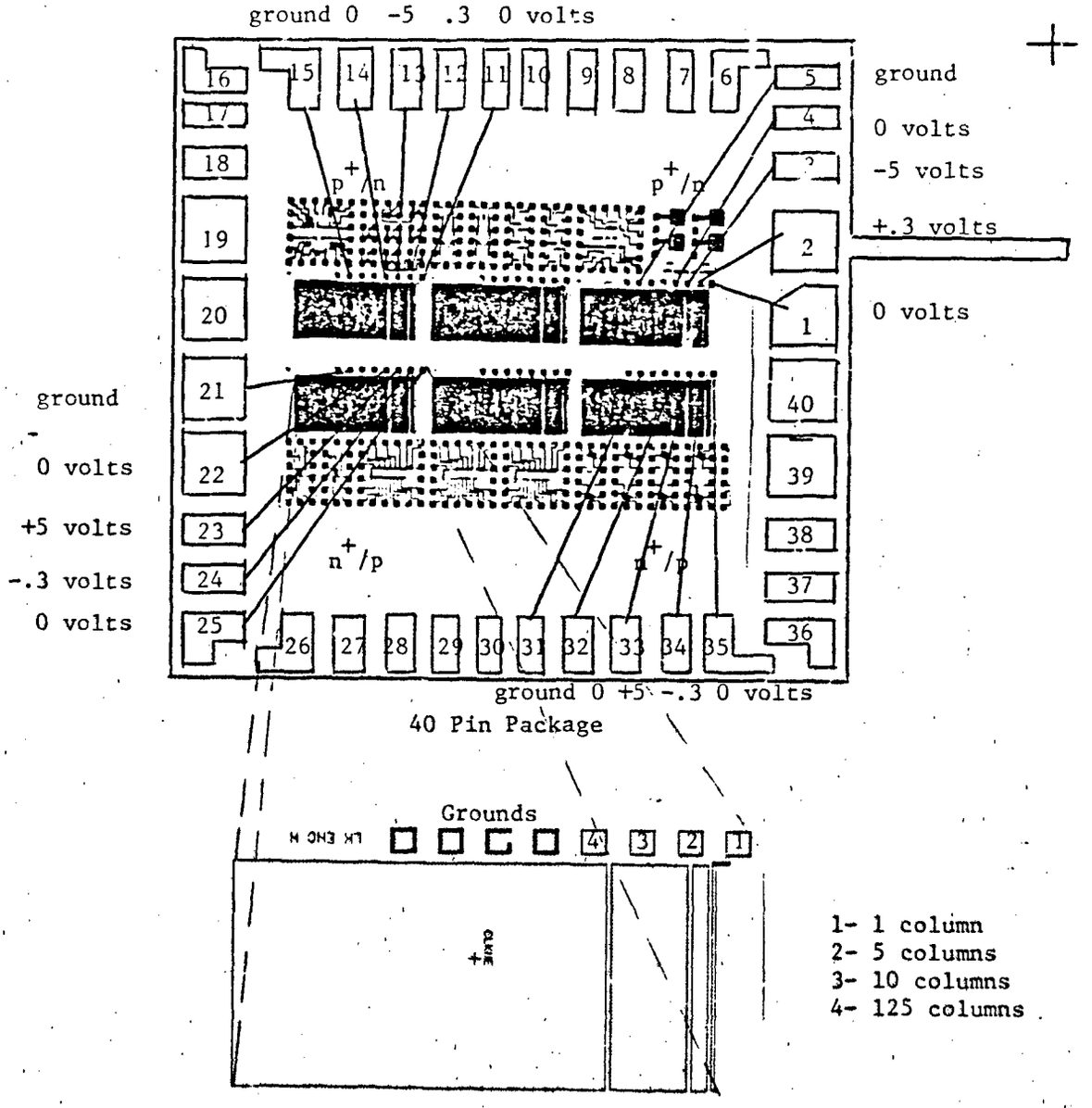


Fig. 1- The diode mask is shown in the package. The experimental biases are given next to the corresponding pins. The inset is an enlarged view of one of the structures showing four sizes of diodes each having 76 contacts per row.

CONTACT GEOMETRIES

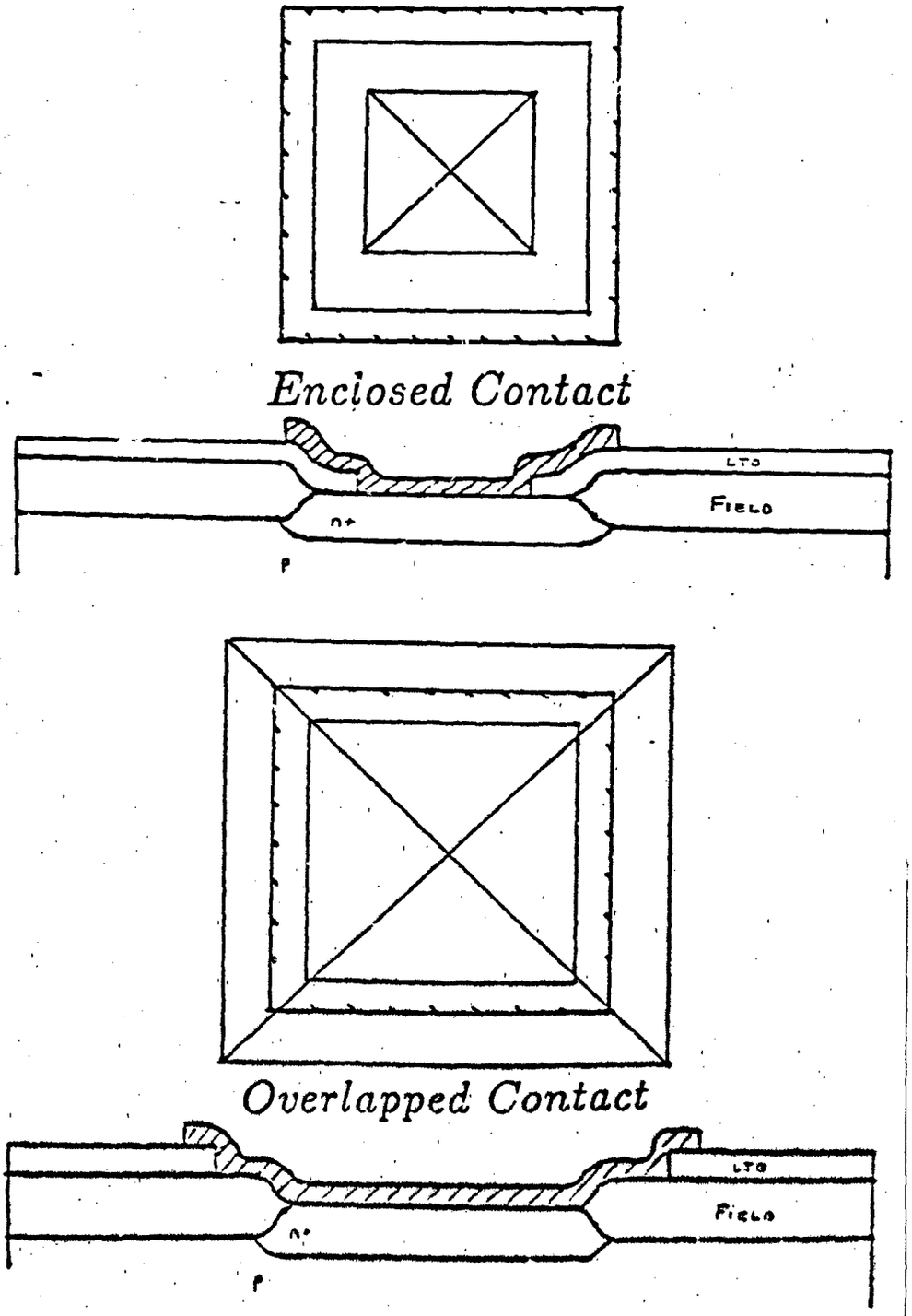


Fig. 2- Clearly shown in plane view and cross section are the two types of contacts used in the experiments

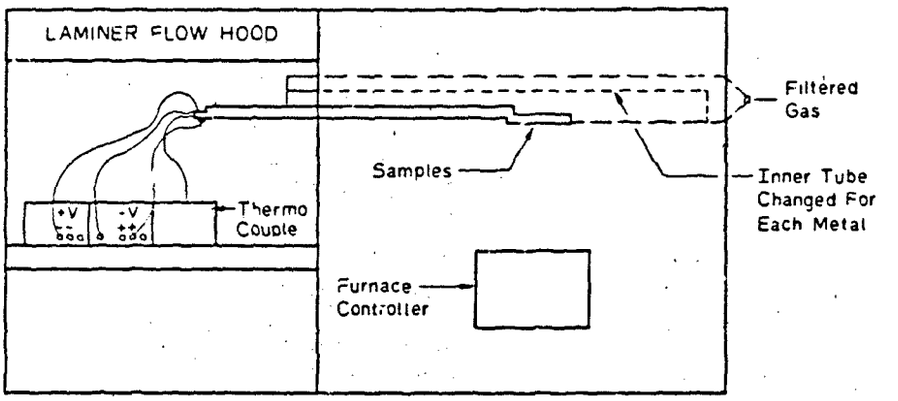


Fig. 3(a)- Experimental set up

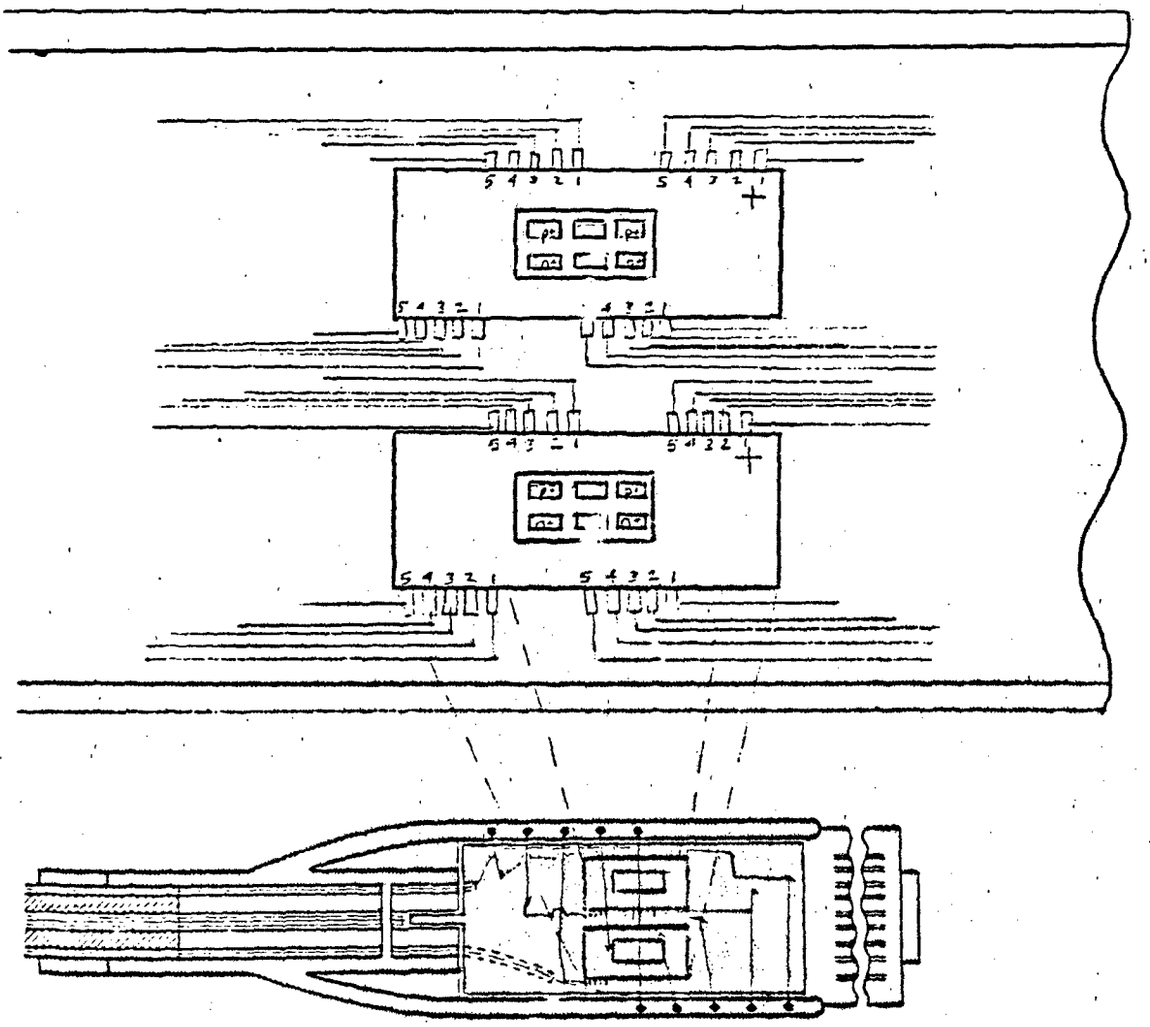


Fig. 3(b)- Connections and package location on the boat are shown. The biases are as shown in Fig. 1.

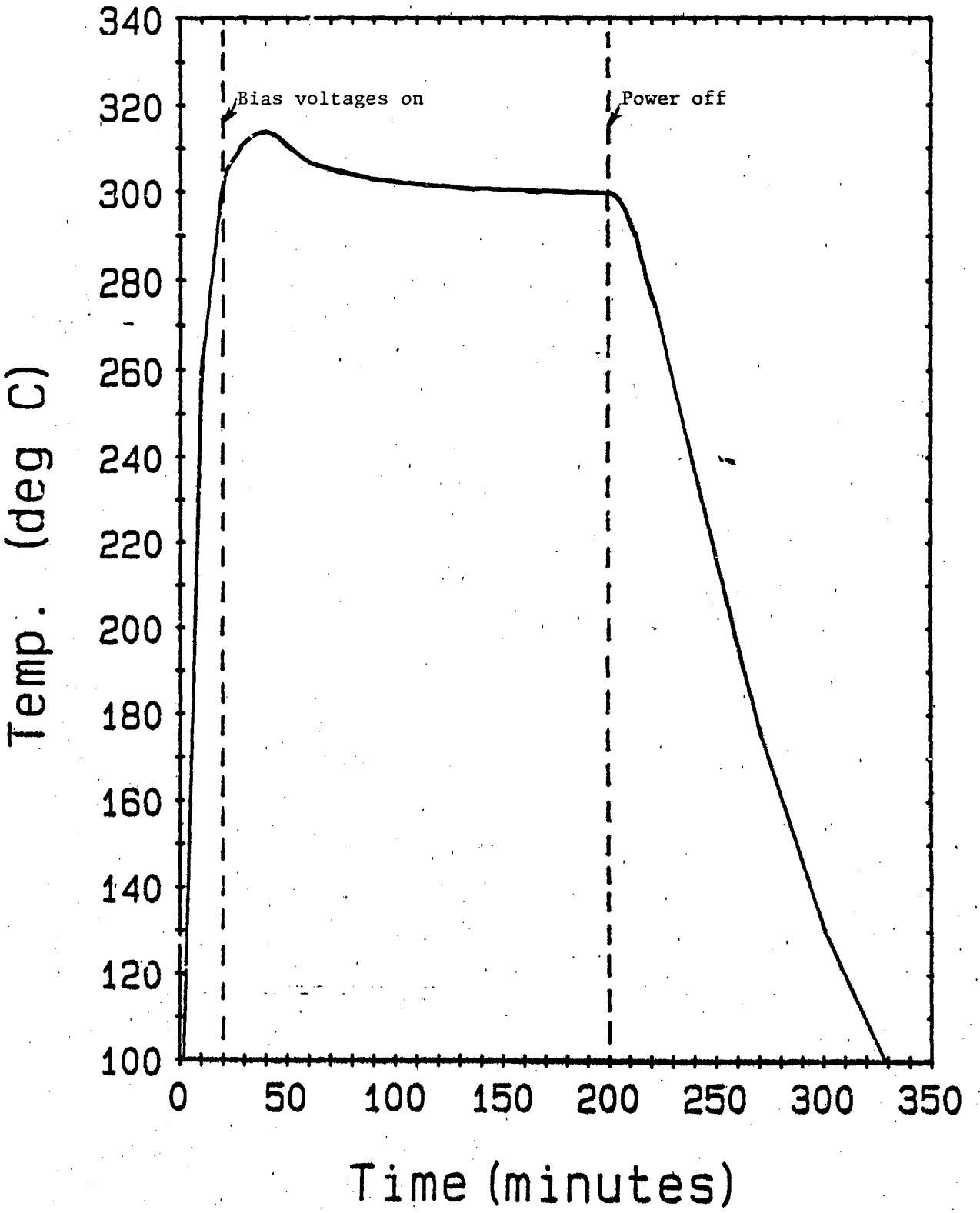
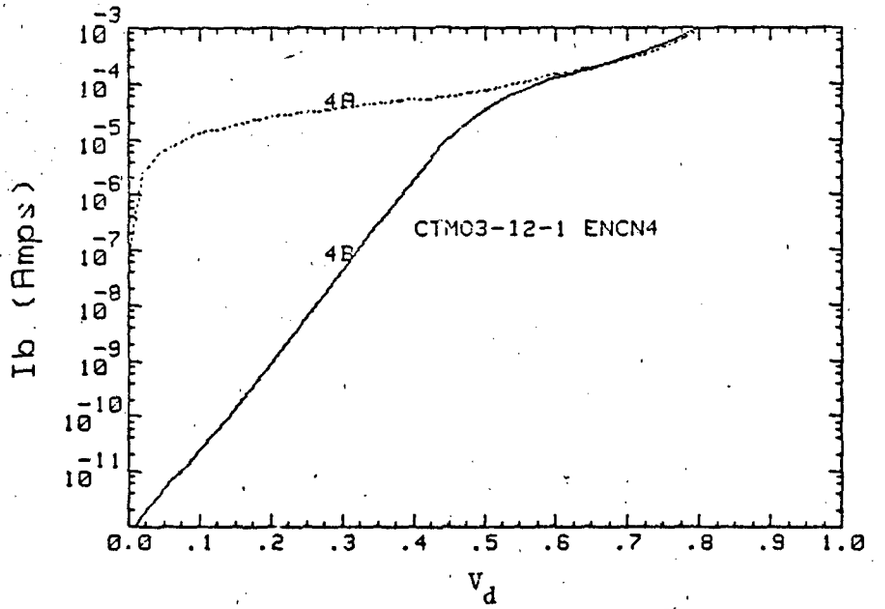
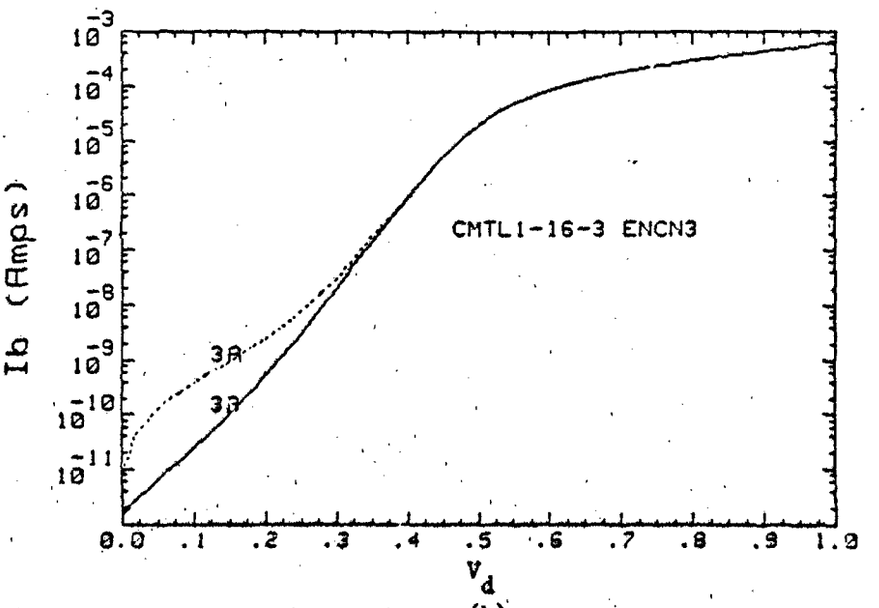


Fig. 4- Time vs. Temperature for a typical experiment

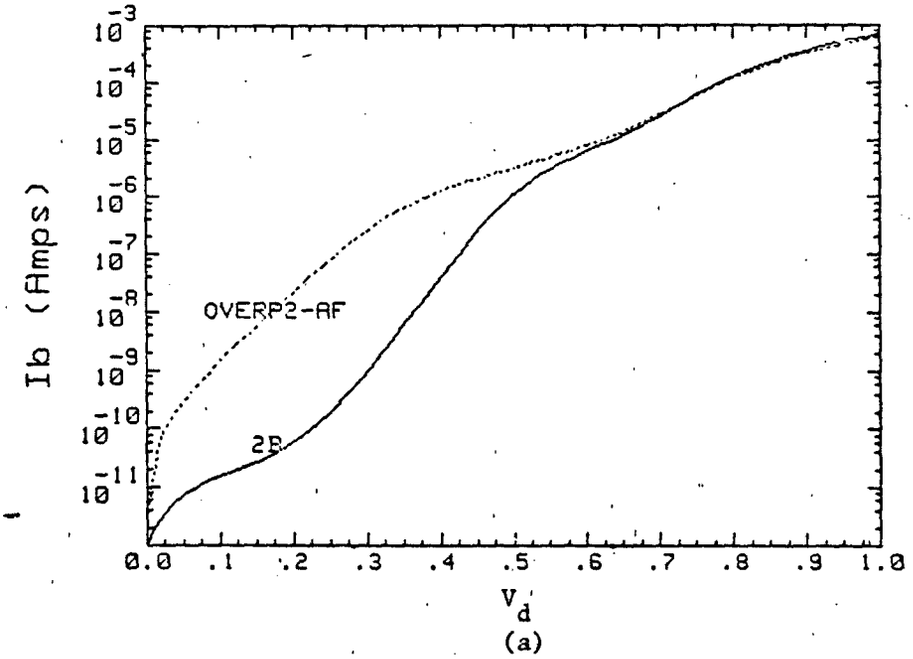


(a)



(b)

Fig. 5- In (a) the results for an enclosed aluminum n^+/p diode are given for before (4B) and after (4A) BJTS. Note that spiking of the junction has occured. In (b) the Pt result is shown for the same structure.



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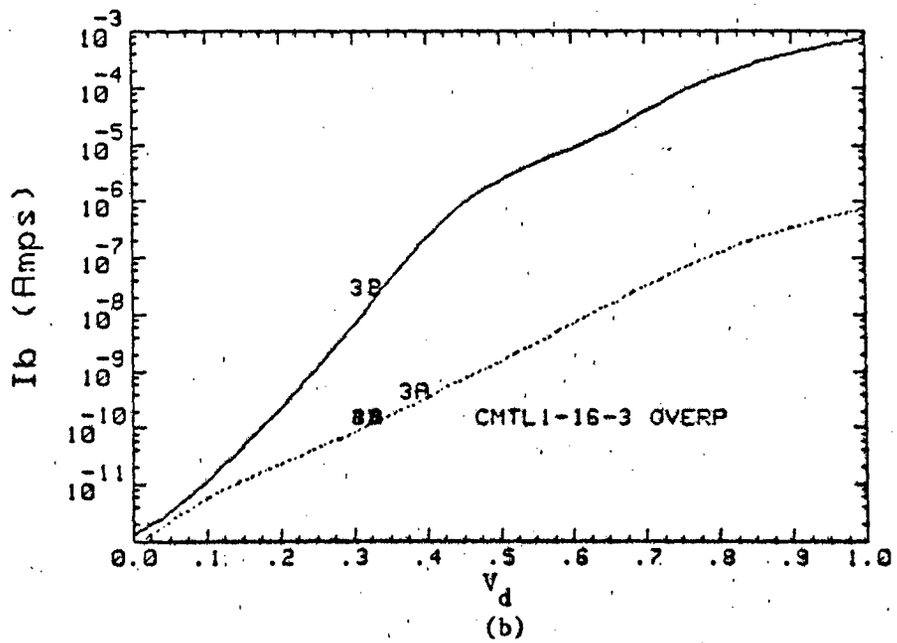
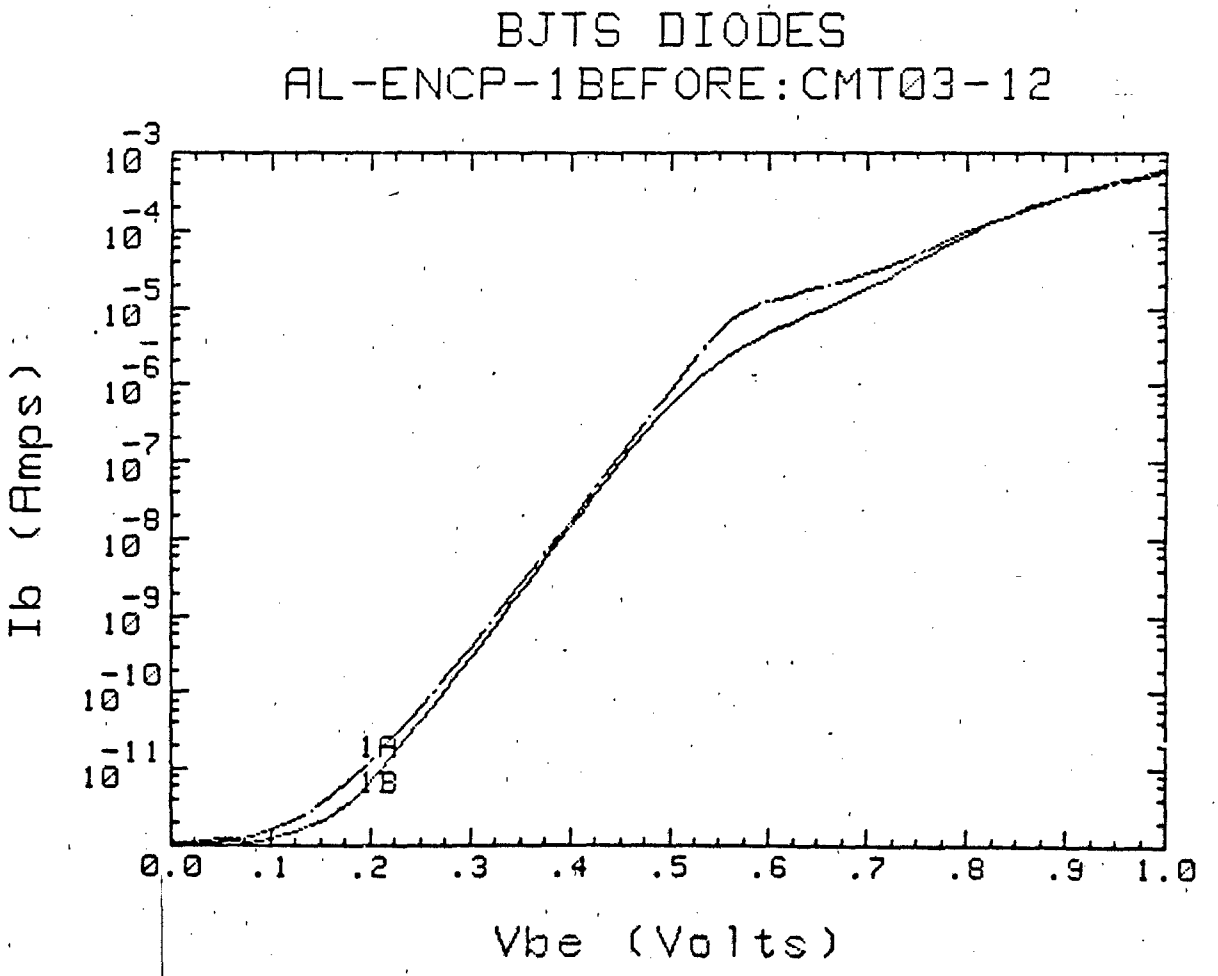


(b)

Fig. 6- In (a) the forward bias aluminum result is shown. All other aluminum results showed no failure after BJTS. In (b) the high resistance of the Pt overlapped structure is evident.



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